

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS</b>  <b>LIST OF REFERENCES</b>	Attorney Docket No. 2885/96	Serial No. 10/551,891
	Applicant(s) VORBACH	
	Filing Date August 28, 2006	Group Art Unit 2183

#### U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,298,043	October 2, 2001	Mauger et al.			
	5,339,840	January 15, 2002	Kothari et al.			
	6,449,283	September 10, 2003	Chao et al.			
	6,681,388	January 20, 2004	Sato et al.			
	7,036,114	April 26, 2006	McWilliams et al.			
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#### FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	WO 07/30395	March 15, 2007	PCT				

#### OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Bondalapati et al., "Reconfigurable Meshes: Theory and Practice," Dept. of Electrical Engineering-Systems, Univ. of Southern California, April 1997, Reconfigurable Architectures Workshop, International Parallel Processing Symposium, 15 pages.
	Cherbaka, Mark F., "Verification and Configuration of a Run-time Reconfigurable Custom Computing Integrated Circuit for DSP Applications," Thesis: Virginia Polytechnic Institute and State University, July 8, 1996, 106 pages.
	Cong et al., "Structural Gate Decomposition for Depth-Optimal Technology Mapping in LUT-Based FPGA Designs," Univ. of California, ACM Transactions on Design Automation of Electronic Systems, Vol. 5, No. 2, April 2000, pp. 193-225.
	FOLDDOC, The Free On-Line Dictionary of Computing, "handshaking," online 13 January 1995, retrieved from Internet 23 January 2011 at <a href="http://foldoc.org/handshake">http://foldoc.org/handshake</a> .
	Li et al., "Hardware-Software Co-Design of Embedded Reconfigurable Architectures," Los Angeles, CA, 2000, ACM, pp. 507-512.
	Marshall et al., "A Reconfigurable Arithmetic Array for Multimedia Applications," FPGA '99 Proceedings of the 1999 ACM/SIGDA Seventh International Symposium on Field Programmable Gate Arrays, 10 pages.
	Pistorius et al., "Generation of Very Large Circuits to Benchmark the Partitioning of FPGAs," Monterey, CA, 1999, ACM, pp. 67-73.
	Translation of DE 101 39 170 by examiner using Google Translate, 10 pages.
EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	